## DETAILED ACTION

Claims 1-15 are present within this instant examination.

### *Priority*

Acknowledgment is made that no priority is claimed for this application and as such the filing date, 8/6/2003, is being used for this examination.

### *Drawings*

Acknowledgment is made that the drawings are accepted since there do not appear to be any issues that would require an objection and/or correction.

### *Response to Arguments*

Applicant's arguments, see page 2, filed 12/06/2007, with respect to claims 1-15 have been fully considered and are persuasive. The 35 U.S.C. 112, first and second paragraph rejections and 35 U.S.C. 103(a) rejections of claims 1-15 has been withdrawn. Examiner notes that on page 2 within applicant's remarks applicant incorrectly referenced page 12 line 20 to page 13 line 4 of the specification, wherein applicant intended to reference page 13 line 19 to page 14 line 4 of the specification which pertains to the dummy match row, layout parasitics, and the match lines.

### *Allowable Subject Matter*

The following is an examiner's statement of reasons for allowance:

Claims 1-15 are allowable.

The present invention pertains to an electric memory test structure having a memory array comprising both a dummy match row and dummy match column. The present invention recites features such as: "... A dummy match row unit coupled to the

memory array and configured to match layout parasitics of match lines of the memory cells; A dummy match column having dummy match cells coupled to the memory array through the match lines, said dummy match column being configured so as to match bitline loading of the memory cells during a search; A dummy timing circuit coupled to the dummy match column and to the dummy match row, said dummy timing circuit being configured to always generate a miss on a dummy match line during the search; and A dummy match control circuit coupled to the dummy timing circuit."

None of the prior art, either taken by itself or in any combination, would have anticipated or made obvious the following limitations within the above limitations at or before the time the invention was filed: " A dummy match row unit coupled to the memory array and configured to match layout parasitics of match lines of the memory cells; A dummy timing circuit coupled to the dummy match column and to the dummy match row, said dummy timing circuit being configured to always generate a miss on a dummy match line during the search; and A dummy match control circuit coupled to the dummy timing circuit."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN D. RADOSEVICH whose telephone number is (571)272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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